CLOCKED DAC CURRENT SWITCH

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CROSS-REFERENCE TO RELATED APPLICATION

Reference is made to the copending U.S. Patent Application entitled "Clocked D/A Converter" by Todd Kaplan, assigned to HRL Laboratories, LLC, Attorney Docket No. B-4850 620354-1, filed on the same date of the present application, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to electrical and electronic circuits and systems. More specifically, the present invention relates to systems and methods for current switching within digital to analog converters.

Description of the Related Art

Currently 'oversampled' delta-sigma ($\Delta\Sigma$) modulator type analog-to-digital (ADC) converters are used for applications requiring accurate conversion of analog signals to digital signals at high speed. As is known in the art, a $\Delta\Sigma$ ADC (also known as a sigma-delta modulator ADC) typically includes an integrator in front of a quantizer. The quantizer provides a digital staircase approximation of the analog input signal. A delta sigma modulator with multibit feedback uses single bit feedback. In this case, the quantizer is typically a single comparator. Further, a $\Delta\Sigma$ ADC

includes one or more feedback loops, which include multi-bit (or single bit) feedback DACs, to avoid the accumulation of quantization errors and to stabilize the $\Delta\Sigma$ ADC.

Delta-sigma modulators allow for the use of low-resolution components running at a higher sampling rate to provide a high resolution ADC converter at a lower sampling rate. Delta-sigma modulators allow for lower costs and higher accuracy than could otherwise be achieved without a delta-sigma modulator. (True, but of limited relevance to the subject of the patent application) Sigma-delta modulator (ADC) converters include a delta-sigma modulator and a digital filter, which processes the output thereof.

A highly precise current switch is needed for current switching of continuous-time analog to digital converters (ADCs) employed in delta-sigma modulators. A simple differential pair of transistors driven by a clocked latch has been used in the past to provide current switching for ADCs used in delta-sigma modulators. However, simple differential pair current switches may be sensitive to thermal history and produce an effect known as 'intersymbol interference'). That is, if the latch has been switched to one state for a sufficient period of time, one transistor heats more than the other and changes its switch threshold. When the signal driving the switch has a non-zero risetime This has the effect of changing the timing of the switch transition. Such thermal errors are difficult to characterize and compensate for.

Traditional approaches for suppressing intersymbol interference include a return-to-zero (RZ) configuration where the DAC current is gated off during part of each clock cycle. However, this requires faster operation of the DAC switch, adds another data edge that is subject to clock jitter, and produces a much less smooth output.

More recently, Adams *et al* described a scheme with two interleaved RZ DACs to provide a more continuous output than does a single RZ DAC. This approach

consumes additional current, is subject to clock jitter, and does not cancel all thermal effects.

A co-pending Application entitled "Clocked D/A/Converter," filed January 21, 2004 (Attorney Docket No. B-4850 620354-1) by Todd Kaplan and Albert Cosand, the teachings of which are hereby incorporated herein by reference, describes a latch used as a DAC switch. Unfortunately, in its simplest form, this circuit is sensitive to the voltage swing at the output summing nodes. This sensitivity can be alleviated by the addition of a common-base output stage, but that may increase the required supply voltage.

Inasmuch as the ADC is typically used in continuous time feedback loop, the timing errors become errors in the analog signals output from the ADC.

Hence, a need remains in the art for a precise switch for use in applications such as a feedback digital to analog converter in a continuous time sigma-delta or delta-sigma modulator.

SUMMARY OF THE INVENTION

The need in the art is addressed by the switch of the present invention. In the illustrative embodiment, the inventive switch includes a first circuit responsive to a first set of complementary input signals for providing complementary output signals; a second circuit responsive to a second set of complementary input signals for providing complementary output signals; and a third circuit for selectively activating the first circuit or the second circuit in response to a control signal.

In a specific illustrative embodiment, the first set of complementary input signals is provided by a master latch and the second set of complementary input signals is provided by a second latch, slaved to the master. The specific illustrative embodiment further includes a first differential pair of transistors having first and

second transistors Q1 and Q2, respectively, and a second differential pair of transistors having third and fourth transistors Q3 and Q4, respectively. The outputs from the master latch are inputs to the first differential pair and the outputs from the slave latch are inputs to the second differential pair. A third differential pair is used to select whether the first differential pair or the second differential pair drives the outputs of the switch. The third differential pair is controlled by complementary clock signals and switches current from a current source in response thereto.

In the illustrative application, the invention is incorporated into a delta-sigma modulator and provides a DAC switch which is insensitive to its thermal history. That is, the inventive switch may be expected to suppress intersymbol interference errors that can result from switching time variations due to a variety of causes, including transient thermal shifts in switching threshold at the switch or in offset of the circuit that drives the switch, or long settling time constants in the switch driver, etc.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an illustrative embodiment of the switch of the present invention is an illustrative delta-sigma modulator application.

Fig. 2 is a timing diagram illustrating the operation of the switch of the present invention.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a circuit diagram showing an illustrative embodiment of the switch of the present invention in an illustrative delta-sigma modulator application. The modulator 10 includes a loop filter 12 of conventional design and construction. As is common in the art, the loop filter 12 is an active filter with transconductors and integrators (not shown). The loop filter 12 provides noise shaping of an input signal. That is, the loop filter 12 shapes the quantization noise in the input signal to a minimum at a frequency at which the modulator will operate.

The loop filter provides complementary outputs which are input to a clocked comparator 14. The comparator 14 ascertains whether the outputs of the filter 12 are positive or negative and provides complementary digital outputs Q and Q-bar in response thereto. The digital outputs from the comparator 14 are input to a master latch 16. The master latch 16 provides differential voltage outputs complementary signals DM and DMX and thereby drives a slave latch 18. The slave latch 18 provides differential voltage outputs DS and DSX. Thus, if the output of the comparator goes to Q, then, assuming a clock with a 50% duty cycle, ½ clock cycle later, the master latch 16 goes to its Q state and ½ clock cycle later, the slave latch goes to its Q state.

The outputs of the master and slave latches 16 and 18 provide inputs to first and second differential pairs Q1/Q2 and Q3/Q4 of the switch 20 of the present invention. In the illustrative embodiment, NPN technology is employed. However,

those skilled in the art will appreciate that PNP or FET technology may be employed as without departing from the scope of the present teachings.

The first and second transistors Q1 and Q2 of the first differential pair are coupled in a common emitter configuration as are the second and third transistors Q3 and Q4 of the second differential pair. The base of each transistor is fed by an output from an associated latch. That is, the DM signal from the Q output of the master latch 16 provides an input at the base of Q1, the DMX signal from the Q-bar output of the master latch 16 provides an input at the base of Q1, the DS signal from the Q output of the slave latch 18 feeds the base of Q3 and the DSX signal from the slave latch 18 feeds the base of Q4. The complementary outputs of Q1 and Q2 are input to the loop filter 12 in common with the complementary outputs of Q3 and Q4.

The switch 20 includes a third differential pair Q5/Q6 which serve to route current from a current source 30 to the first or the second differential pair Q1/Q2 and Q3/Q4 in response to a complementary clock signal from a clock 40. The collector of Q5 is coupled to the common emitter of Q5 and Q6. The collector of Q6 is coupled to the common emitter of Q3 and Q4. The common emitter of Q5 and Q6 is connected to the current source 30. In the illustrative embodiment, the current source is implemented as a cascode current source with a first transistor Q7 connected in cascode with a second transistor Q8. The transistor Q8 is connected to a source of negative potential via a resistor R1.

Thus, a continuous feedback path is provided to the loop filter 12 and the data fed back determines whether the feedback signal is positive or negative. As is known in the art, a 'continuous time' DAC (digital-to-analog converter) in one in which data is being output continuously up to the time of switching. Fig. 2 is a timing diagram illustrating the operation of the switch of the present invention. The inputs are three differential signal pairs: the clock CLK/CLKX, and two copies of the data, DM/DMX and DS/DSX. As seen in Fig. 2, the two versions of the data differ in delay by one

half of a clock period; DM and DS may be obtained respectively from the master and slave latches of a D flip-flop. DM changes state following a falling edge of CLK and DS changes state following a rising edge of CLK. As mentioned above, the differential pair Q1/Q2 is driven by the master latch output DM. The logic signal at the bases of Q1 and Q2 has had a half clock period to settle when CLK goes high and causes the DAC tail current to be steered through Q5 into the emitters of Q1/Q2. The current is then steered to the selected output according to the state of DM. During the time that CLK is high, DS has time to settle to its correct value so that when CLK goes low (CLKX goes high) the DAC current will be steered through Q6 to the emitters of Q3/Q4 and then to the correct output.

Small variations in the transition time of the data signals should have no effect on the timing of the current output of the overall DAC switch, inasmuch as the timing is determined by the clock after the data is settled.

Thus, the present invention provides a current switch for a digital to analog converter in which the timing of the current switching is controlled by a clocking signal and not by the data signal that determines which way the current is switched. The relative timing of the clock and data signals is such that the data is allowed to fully settle before the clock gates the DAC current to the differential pair controlled by the data. Two data switches gated by opposite phases of the clock are provided so that the current output waveform is equivalent to a single DAC switch driven by an NRZ data signal.

The signal to the upper differential pair, DM and DMX or DS and DSX, settles to its full steady state before current is switched into the emitters of the differential pair through the clock transistor. Thus, the signal at one pair is changing while the current is switched through the other pair. After the signal has settled, the clock goes high and current is steered through the DM pair driven by the master. While the current is flowing through the pair driven by the master, the inputs to the pair driven by the slave

have a chance to settle as no current is flowing therethrough. After the inputs have settled, then the clock switches current through that pair. Hence, the inputs are allowed to settle to a full logic value before current is switched to the emitters of the differential pair. This prevents slight variations in timing from influencing the output.

Although the invention was described in the context of an illustrative delta-sigma modulator application, those skilled in the art will appreciate that the present teachings are not limited thereto. The present teachings may be employed in any application requiring a continuous time digital to analog conversion. That is, in some applications, the loop filter and the comparator may be eliminated and the master and slave latches driven directly. In this case, the outputs of the first and second differential pair serve as the output of the circuit.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS